APPLICATION NOTE

ABSTRACT
This application note describes a practical method that allows a member of the LPC family of microcontrollers to be programmed while mounted in the end product.

AN466
In-system programming of the P87LPC76x family of microcontrollers

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INTRODUCTION

The P87LPC76x microcontroller family is programmed serially, which allows you to do in-system programming. For example, address and data used to program the device are sent in a serial format on two-wires. Device configuration is done via this same interface. This application note discusses how to use the serial programming while mounted in the end product.

IN SYSTEM PROGRAMMING

Since only 5 pins are required to program members of the LPC family, it is practical to design an interface that allows a member of the P87LPC76x family to be programmed after it is soldered in the final product. Programming a device after it is soldered on a circuit board has many advantages including:

- The latest software revision can be loaded into the product just prior to shipment.
- The 32 byte customer data area of the EPROM on the LPC can be programmed to have unique serial numbers or calibration data, etc.
- The handling, which can damage the device is eliminated.
- Software can be used to differentiate between products which share a common hardware design.

The basic approach is simple. As shown in Figure 1, a standard commercial programmer is connected to the system board via a 5 wire cable. One end of the cable has a header, which fits into the programmer's ZIF socket while the other end plugs into the circuit board. Connection to the device pins are shown below. In this example, the application is isolated from the device during programming. If the application cannot be isolated, then the programmer must be able to drive the impedance created by the application and the device to be programmed. If the programmer cannot drive the circuit to the voltage levels within the time required by the device being programmed, the programmer output will require buffering. Care needs to be taken to make sure that the application is not damaged during the programming.

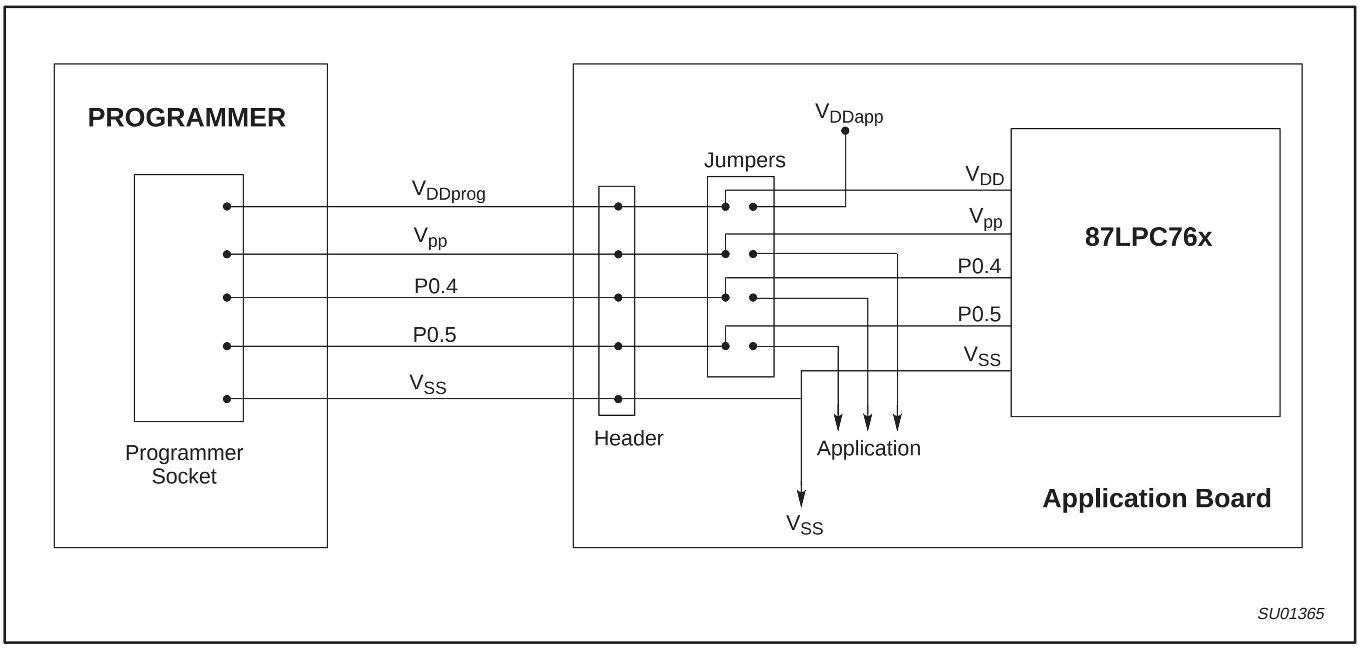

Figure 1. Programmer Connection

The signals that connect the programmer to the board are given in Table 1 .

Table 1. Programmer Connections

Function	Pin Number			Break Normal Connection?
	20 pin pkgs	16 pin pkgs	14 pin pkgs	
V_{SS}	5	4	3	No
P1.5 / RST / V_{PP}	4	3	2	Yes[1,3]
P0.4 / Alt Function(s) / Programming Data / Programming Address	17	14	13	Yes[1]
P0.5/Alt Function(s)/Programming Clock	16	13	12	Yes[1]
V_{DD}	15	12	11	Yes[2]

NOTES:

1. The connections do not have to be broken when the programmer can drive the part and application to a "1" or "0" while programming and when the part can drive the application to "1" or "0" when the program is verified by the programmer, but this is not recommended.
2. The connection to V_{DD} does not have to be broken when the programmer and application-board have the same V_{DD}.
3. V_{PP} is 10.75 V. If this pin is not isolated from the application, the application must be able to withstand this voltage.

Note: The alternative functions on P0.4 and P0.5 vary between different members of the P87LPC76x family.

A few precautions need to be taken when designing a board that allows a member of the 87LPC76x family to be programmed once it is soldered in place.

SIGNATURE BYTES

Each member of the P87LPC76x contains three signature bytes that can be read and used by the programming system to identify the device being programmed. The code contained in the signature bytes for the devices in the family are shown in Table 2.

Table 2. Signature Bytes

Device	Address FC30 h	Address FC31 h	Address FC60 h	Program Memory
P87LPC760	15 h	DD h	07 h	1 kbyte
P87LPC761	15 h	DD h	06 h	2 kbytes
P87LPC762	15 h	DD h	03 h	2 kbytes
P87LPC764	15 h	DD h	00 h	4 kbytes
P87LPC767	15 h	DD h	01 h	4 kbytes
P87LPC768	15 h	DD h	04 h	4 kbytes
P87LPC769	15 h	DD h	02 h	4 kbytes

The signature byte codes for future members of the family will be included in the data sheets for each device as it is introduced. The signature bytes may be read by the user program by placing the address indicated above in the DPTR and using a MOVC instruction.

Customer Data Area

Inside the EPROM there are 32 bytes reserved for fixed data. This block starts at address FCE0 h and ends at FCFF h. Since this data exists in the code memory space, it can be accessed by placing the desired address in the DPTR and using the MOVC instruction. Typical contents of these locations might include code revision identification, checksum storage, or a unique serial number for each device. These locations can be programmed at the same time as the rest of program memory and configuration bytes.

System Configuration Bytes

A number of user configurable features of the P87LPC76x family must be defined before power is applied to the device. As a result they cannot be set by the user's program. These functions are enabled by programming UCFG1 located at FD00 h and UCFG2 located at FD01 h. These bytes can be programmed at the same time as the rest of the memory. A MOVX instruction can be used to read these locations. The control register formats are shown in the following two figures.

Table 3. User Configuration Register 1

UCFG1 ADDRESS FD00 H **UNPROGRAMMED VALUE FF H**

7	6	5	4	3	2	1	0
WDTE	RPD	PRHI	BOV	CLKR	FOSC2	FOSC1	FOSC0

BIT	SYMBOL	FUNCTION
UCFG1.7	WDTE	Watchdog Timer Enable. When “1” watchdog is enabled;. A “0” disables watchdog, however the timer may still be used to generate an interrupt.
UCFG1.6	RPD	Reset Pin Disable. A “1” disables the reset function on pin P1.5 allowing its use as an input only pin. A “0” enables the reset function on pin P1.5.
UCFG1.5	PRHI	Port Reset High. When “1” a reset causes ports to be initialized high, when “0” reset causes the ports to be initialized low.
UCFG1.4	BOV	Brownout Voltage Select. When “1”, the brownout detect voltage is 2.5 V, when “0” it is 3.8 V.
UCFG1.3	CLKR	Clock Rate Select. When “0” the processor operates with the standard 80C51 12 clock cycles per machine cycle, when “1” there are 6 clock cycles per machine cycle.
UCFG1.2–UCFG1.0	FOSC2–0	CPU oscillator type select. Combinations other than those shown below should not be used.
	1 1 1	External clock input on X1. (Default on unprogrammed device)
	0 1 1	Internal RC Oscillator, 6 Mhz (see datasheet for tolerance)
	0 1 0	Low frequency crystal or resonator, 20 kHz to 100 kHz.
	0 0 1	Medium frequency crystal or resonator, 100 kHz to 4 MHz.
	0 0 0	High frequency crystal or resonator, 4 Mhz to 20 MHz.

Table 4. User Configuration Register 2

UCFG2 ADDRESS FD01 H **UNPROGRAMMED VALUE FF H**

7	6	5	4	3	2	1	0
SB2	SB1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

BIT	SYMBOL	FUNCTION
UCFG2.7–UCFG2.6	SB2–1	Security Bits 2–1. Function described below.
	1 1	No security features enabled. EPROM can be programmed and verified.
	1 0	Further EPROM programming disabled; verify enabled.
	0 1	This combination is not supported.
	0 0	All EPROM verification and programming disabled.

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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